IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A quantizer for a sigma delta modulator [[with]] having at least one input stage providing an input signal to the quantizer, the quantizer quantizing [[an]] the input signal, ~~which is present at its input stage,~~ in accordance with at least one threshold signal and outputting [[it]] the quantized input signal as a digital result value at a digital result output of the sigma delta modulator, characterized in that

the quantizer contains at least one quantizing cell ~~corresponding~~ wherein the number of quantizing cells corresponds to the number of [[its]] the resolution levels of the quantizer, each quantizing cell having an input voltage/current converter ~~, which converts~~ for converting the input signal to be quantized into a corresponding input signal current~~, to the at least one quantizing cell,~~ ;

a static threshold current source is allocated to the at least one quantizing cell, the static threshold current source supplying ~~which supplies~~ a static component to the threshold signal in the form of a static threshold current~~,~~ ~~that~~;

wherein the quantizing cell comprises a dynamic feedback current source ~~is provided~~ which generates [[a]] an analog feedback current derived from the digital result value, [[which]] wherein the analog feedback current is added to the static threshold current in a current node [[, that]] ;

wherein the threshold current is composed of the static threshold current and the feedback current is added to the input signal current in the current node ~~,~~ ~~that~~ ;

wherein the quantizing cell includes a comparison unit ~~is provided which decides whether the accurate~~ coupled to the current node for detecting whether the summed up current ~~present~~ at the current node is not equal to zero and ~~supplies~~ for outputting a digital quantizer cell result accordingly; and

wherein the digital quantizer cell results form the digital result value.

2. (Currently Amended) The quantizer as claimed in claim 1, wherein ~~, for obtaining~~ the analog feedback current is derived from the digital result value [[,]] by a digital/analog converter ~~is provided which supplies a~~ supplying an analog voltage signal corresponding to the digital result value ~~for deriving the feedback current~~.

3. (Currently Amended) The quantizer as claimed in claim 2, wherein the digital/analog converter is constructed in such a manner that it supplies the analog feedback current directly as its analog output signal.

4. (Currently Amended) The quantizer as claimed in claim 1, wherein the input voltage/current ~~of the current~~ converter is a transistor driven at a base input by means of the input signal.

5. (Previously Presented) The quantizer as claimed in claim 1, wherein each quantizing cell is allocated a threshold signal which differs from the threshold signals of other quantizing cells.

6. (Previously Presented) The quantizer as claimed in claim 1, wherein the threshold signals exhibit fixed differences with respect to one another.

7. (Currently Amended) The quantizer as claimed in claim 1, wherein an amplifying stage is provided which amplifies the current at the current node before it is ~~weighted by~~ fed to the comparison unit.

8. (Previously Presented) The quantizer as claimed in claim 1, wherein a latch is provided as comparison unit.

9. (Currently Amended) The quantizer as claimed in claim 1, wherein the latch ~~exhibits~~ comprises a comparator and a sample-and-hold device.

10. (Previously Presented) The quantizer as claimed in claim 1, wherein the quantizer is constructed symmetrically with a positive and a negative signal path and correspondingly with a positive signal input for a positive input signal and with a negative signal input for a negative input signal.

11. (Previously Presented) The quantizer as claimed in claim 8, wherein a degeneration resistor is provided between a positive and a negative signal path.

12. (Previously Presented) The quantizer as claimed in claim 1, wherein a separate static threshold current source is allocated to each quantizing cell.

13. (Currently Amended) A quantizer for a sigma delta modulator [[with]] having at least one input stage providing an input signal to the quantizer, the quantizer quantizing [[an]] the input signal, ~~which is present at its input stage,~~ in accordance with at least one threshold signal and outputting [[it]] the quantized input signal as a digital result value [[at]] to a digital result output of the sigma delta modulator, wherein the quantizer contains at least one quantizing cell, the number of quantizing cells corresponding to the number of [[its]] the resolution levels of the quantizer, each quantizing cell ~~exhibiting~~ comprising a voltage comparator which compares the input signal, present as an input signal voltage [[,]] with an associated threshold signal voltage and, if the input signal voltage exceeds or drops below the threshold signal voltage, outputs a corresponding digital result bit, wherein the result bits form the digital result value,

a digital adder being provided which adds the digital result value [[of]] corresponding to [[the]] last ~~weighting~~ output of the comparators of the quantizer to each of the ~~individual~~ threshold signal voltages [[of]] associated to the comparators by incrementing or decrementing the respective threshold signal voltages by [[part]] partial voltages corresponding to the digital result value.

14. (Currently Amended) The quantizer as claimed in claim 13, wherein a threshold signal is allocated to each quantizing cell, ~~a threshold signal is allocated which differs~~ the threshold signal being different from the threshold signals of other quantizing cells.

15. (Currently Amended) The quantizer as claimed in claim 13, wherein a reference voltage generator is provided which generates the threshold signal voltages, which are different for each voltage comparator, the threshold signal voltages being selectable in [[part]] partial voltages.

16. (Currently Amended) The quantizer as claimed in claim [[13]] 15, wherein the reference voltage generator ~~is constructed by~~ comprises a chain of resistors~~, the part voltages of which are assembled to form the threshold voltages~~.

17. (Currently Amended) The quantizer as claimed in claim [[13]] 15, wherein a switching ~~mechanism~~ apparatus is allocated to the adder, [[which]] the switching ~~mechanism exhibits~~ apparatus comprising switches, [[at]] the switching apparatus having inputs [[of]] to which the [[part]] voltages of the reference voltage generator are supplied, ~~present~~ and the switching apparatus having outputs [[of]] which are connected to the inputs of the comparators for the threshold signal voltages ~~of the comparators~~, the switches being controlled by ~~the output~~ a control signal of the adder.

18. (Currently Amended) The quantizer as claimed in claim [[13]] 17, wherein the reference voltage generator generates the [[part]] partial voltages which can be ~~applied to~~ added to the threshold signal voltages of the ~~respective comparator for weighting the input signal~~ comparators in accordance with the digital result value ~~and/or the desired threshold signal voltage~~ by [[means]] use of the switches.

19. (Canceled)

20. (Previously Presented) The quantizer as claimed in claim 13, wherein the threshold signals exhibit fixed differences with respect to one another.

21. (Previously Presented) The quantizer as claimed in claim 13, wherein the quantizer is constructed symmetrically with a positive and a negative signal path and correspondingly with a positive signal input for a positive input signal and with a negative signal input for a negative input signal.

22. (Previously Presented) The quantizer as claimed in claim 13, wherein the comparators are formed by continuous-time voltage comparators.

23. (Previously Presented) The quantizer as claimed in claim 13, wherein a latch is provided which stores the result supplied by the comparators.

24. (Currently Amended) A sigma delta modulator having at least one input stage and [[with]] having a quantizer as claimed in claim 13.